A Two-Step Absorber Deposition Approach To Overcome Shunt Losses in Thin-Film Solar Cells: Using Tin Sulfide as a Proof-of-Concept Material System

A two-step absorber deposition approach to overcome shunt losses in thin film solar cells: using tin sulfide as a proof-of-concept materials system

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Abstract

As novel absorber materials are developed and screened for their photovoltaic (PV) properties, the challenge remains to reproducibly test promising candidates for high-performing PV devices. Many early-stage devices are prone to device shunting due to pinholes in the absorber layer, producing "false negative" results. Here, we demonstrate a device engineering solution towards a robust device architecture, using a two-step absorber deposition approach. We use tin sulfide (SnS) as a test absorber material. The SnS bulk is processed at high temperature (400˚C) to stimulate grain growth, followed by a much thinner, low-temperature (200˚C) absorber deposition. At lower process temperature, the thin absorber overlayer contains significantly smaller, densely packed grains, which are likely to provide a continuous coating and fill pinholes in the underlying absorber bulk. We compare this two-step approach to the more standard approach of using a semi-insulating buffer layer directly on top of the annealed absorber bulk, and demonstrate a more than 3.5x superior shunt resistance R_{sh} with smaller standard error σ_{Rsh}. Electron-beam induced current (EBIC) measurements indicate a lower density of pinholes in the SnS absorber bulk when using the two-step absorber deposition approach. We correlate those findings to improvements in the device performance and device performance reproducibility.

1. Introduction

The rapid performance improvement of lead halide perovskite solar cells has spurred the search for non-toxic, earth-abundant perovskite-inspired photovoltaic (PV) materials.[1–3] To validate the PV potential of these candidates, it remains an important challenge to demonstrate high-performing PV devices. Many early-stage devices based on new-emerging perovskite-inspired absorber materials are prone to device shunting due to pinholes in the absorber layer, caused by unoptimized fabrication processes.[4–6] There is the danger that early-stage low power conversion efficiencies (PCE) due to shunting effects may contribute to "false negative" results. Hence, there is an urgent need to engineer more robust device architectures that allow for rapid PV device performance testing of novel absorbers without sacrificing device performance due to shunting losses. Yokoyama *et al*. have recently introduced a modified vapor assisted solutions processing method for more uniform and pinhole-free thin film fabrication *via* solution.[7] Pinhole treatments in thin films has previously been developed for large area amorphous silicon[8] as well as cadmium telluride solar cells[9].

Tin sulfide is a promising, emerging thin film absorber candidate; tin (Sn) and sulfur (S) are both scalable and non-toxic constituents. The SnS molecule congruently evaporates as one molecule at temperatures below 600˚C, allowing for potentially low manufacturing costs. Due to its high optical absorption coefficient in the visible spectrum (> 10^5 cm^{-1}),[10–12] film thicknesses below 1 μm are sufficient to absorb most of the incident sunlight. Despite its promising PV properties, devices based on SnS are still underperforming compared to the theoretical maximum efficiency of 32%, assuming a bandgap of 1.1 eV.[13] In recent years NREL certified record efficiencies of η = 3.88% and η = 4.36% have been achieved via thermal evaporation (TE) and atomic layer deposition (ALD), respectively.[14,15]

A performance loss analysis of TE SnS solar cells suggests that the device performance and performance reproducibility of TE SnS solar cells is affected by a low shunt resistance R_{sh} (74 Ω cm^2), which reduces the fill factor (FF) and open-circuit voltage V_{OC}.[14] The low shunt resistance might result from pinholes in the SnS bulk and current pathways around the edges of the device.[14] Experimental data of identically fabricated one-step deposition baseline devices indeed reveals a correlation between the shunt resistance and the V_{OC}, as shown in Figure 1. A low R_{sh} < 200 Ω cm^2 limits the V_{OC} potential and reproducibility of the device (see grey-shaded area). For R_{sh} > 200 Ω cm^2, the number of devices with a V_{OC} of (330 ± 30) mV significantly increases. Figure 1 reveals only observe three outliers with a V_{OC} well below 300 mV for R_{sh} > 200 Ω cm^2. Overall, a higher shunt resistance enables a higher V_{OC} and improves performance reproducibility. The trend in experimental data (blue dots) matches the expected trend seen in device simulations (red line), when varying the R_{sh}, using a previously developed optoelectronic model[16] with all other device parameters kept constant at the values used in reference [16]. In addition, calculations predict a 15% relative improvement in the FF and thus in the overall device performance if R_{sh} can be increased to 1000 Ω cm^2.[14] Hence, a simple but reliable approach towards mitigation of shunt losses in early-stage thin film device may allow for rapid material and device evaluation before final device optimization is completed, with a reduced risk of "false negatives" from shunting.

In this work, we investigate the root cause of shunting losses in thin film solar cells and its impact on performance and performance reproducibility. We study SnS thin film substrate-style solar cells. We test the hypothesis that many of our solar cells suffer from a low device shunt resistance due to pinholes in the SnS absorber bulk. We use electron-beam induced current (EBIC) measurements to image through-thickness current pathways in the SnS absorber. We demonstrate a two-step absorber deposition approach that appears to block pinholes and thus improves the shunt resistance R_{sh}. As a result, we observe enhanced solar cell performance and performance reproducibility. This two-step deposition approach is generalizable, and may be applicable to other thin film opto-electronic device structures as a shunt mitigation engineering solution.

The design of a robust thin film device architecture will be essential for our ongoing work on SnS bulk engineering and testing the impact on device performance. The two-step deposition method will allow the use of more conductive buffer layers in substrate-style device configurations. Here, we use tin sulfide as a proof-of-concept materials systems. Device shunting due to pinhole formation has been observed in other polycrystalline thin film materials as well. Novel polycrystalline absorber materials such as antimony selenide (Sb_2Se_3)[27] and copper antimony sulfide ($CuSbS_2$)[28] have been successfully applied in photovoltaic devices. However, shunt resistances have been reported which may limit the device performance to-date. When exploring novel promising classes of materials for thin film device applications (*e.g.*, nitride semiconductors

for solar energy conversion[29]), it will be important to avoid false-negatives due to device shunting. We believe that the here presented two-step absorber deposition approach (in particular the combination of a high-temperature and subsequent low-temperature step) is generalizable, and may be applicable to a variety of novel thin film materials (potentially even beyond photovoltaic applications).

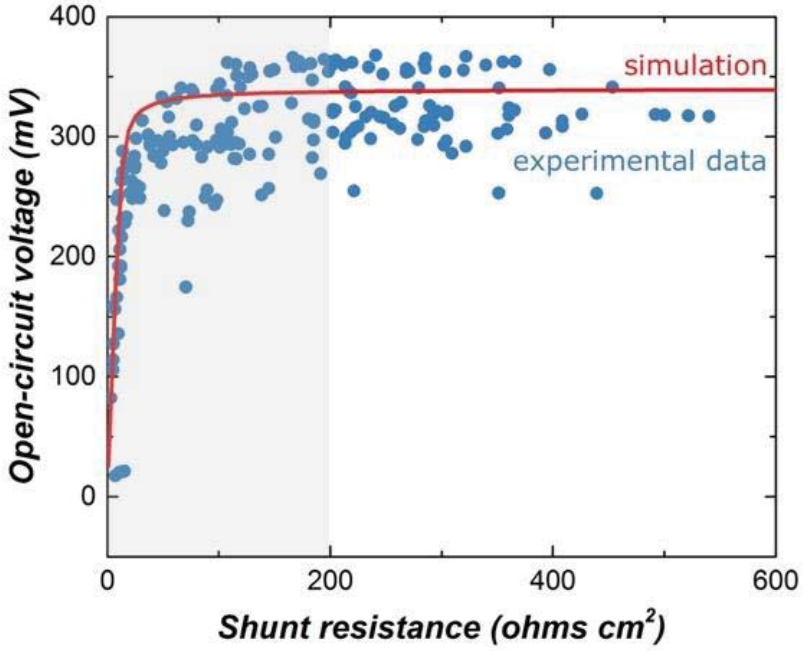

Figure 1 Open-circuit voltage V_{OC} of identically fabricated SnS one-step deposition baseline devices plotted as a function of the illuminated shunt resistance R_{sh}. An increase in R_{sh} leads to an increase in V_{OC} and a smaller standard error in V_{OC}. The trend in experimental data (blue dots) matches the expected trend seen in device simulations (red line), when varying the R_{sh}, using a previously developed optoelectronic model[16] with all other device parameters kept constant at the values used in reference [16]. The grey shaded area highlights the regime of low R_{sh} resulting in low V_{OC}. For $R_{sh} > 200\ \Omega\ cm^2$, the number of devices with a V_{OC} of (330 ± 30) mV significantly increases with the exception of only three outliers showing a V_{OC} well below 300 mV.

2. Experimental Methods

SnS substrate-style devices were fabricated on commercial Si/SiO_2 wafers. The wafers were cleaned in a hot solvent bath and nitrogen-dried prior to the molybdenum (Mo) back contact deposition. The SnS bulk was deposited in a single-source custom-made thermal evaporator at a substrate temperature of 240 ± 30 ˚C. Further details on the back contact and absorber bulk deposition can be found in reference [14]. The SnS bulk was annealed for 60 minutes in 4% H_2S in N_2 at 400˚C, with a total pressure of 28 ± 1 Torr. For the SnS one-step deposition baseline devices, the thermally evaporated SnS thin film was exposed to ambient air for 24 hours to grow a thin SnO_x layer prior to the buffer layer deposition. For the two-step absorber deposition devices, the thermally evaporated SnS thin film was transferred from the annealing furnace to the atomic layer deposition (ALD) chamber. During the transfer the film was exposed to air for less than two

minutes. A second thin SnS absorber layer (75 nm) was grown *via* ALD at 200˚C before applying the same surface oxidation procedure as to the baseline SnS samples. The *n*-type buffer layer was grown *via* ALD at 120˚C on all SnS device samples, comprising 30 nm of nitrogen-doped Zn(O,S) with a S/Zn ratio of 1:14 and 10 nm ZnO. Indium tin oxide (ITO) with a sheet resistance of 40 Ω/sq was sputtered as the transparent top contact, using a shadow mask. Ag fingers and contact pads were deposited *via* e-beam evaporation and used for metallization.

The morphology of the SnS thin films was imaged by field-emission scanning electron microscopy (FESEM, Zeiss, Ultra-55). Cross-sectional EBIC measurements were performed at MIT, using an FEI Helios NanoLab dual-beam system equipped with a Point Electronic DISS 5 EBIC system, at an accelerating voltage of 5 kV and beam current of 86 pA. The device cross-section was polished before the EBIC measurement using argon ion milling (JEOL cross section polisher), at an accelerating voltage of 5 kV and argon flow rate of 6 sccm for 4 hours.

The solar cells were characterized at room temperature (24.9°C) by current density-voltage (*J-V*) and external quantum efficiency (EQE) measurements at MIT, using a Keithley 2400 sourcemeter. The standard illumination of 100 mW cm^{-2} was generated by a Newport Oriel 91194 solar simulator with a 1300 W Xe-lamp using an AM1.5G filter, and a Newport Oriel 68951 flux controller calibrated by a silicon reference cell equipped with a BK-7 window, certified by the National Renewable Energy Laboratory (NREL). The area of each device is 0.27 cm^2, defined by the ITO area. The EQE measurements were performed with a PV Measurements Model QEX7 tool. In addition, a representative SnS baseline device was characterized with and without a light mask (area of 0.22 cm^2) by the cell certification team at NREL. The light mask is used as an additional tool to define the active device area under illumination. Device simulations were performed using a solar cell capacitance simulator (SCAPS).[17] The shunt resistance R_{sh} in the dark and under illumination was derived from the slope of the *J-V* curve at zero voltage.

3. Results and Discussions

3.1.High-temperature treatment of polycrystalline thin films

High-temperature (HT) treatments have been shown to stimulate grain growth in various polycrystalline thin film absorber materials (*e.g.*, CZTS,[18–20], CdTe[21] and lead halide perovskites[22]), contributing to enhanced device performances due to reduced charge carrier recombination losses at grain boundaries. Similarly, we have found HT treatments of the SnS absorber films to result in significant grain growth and increased charge carrier transport properties.[23,24] Figure 2 reveals plan-view and cross-sectional scanning electron micrographs (SEM) comparing small-grained (< 500 nm), as-deposited SnS thin films at 240°C (top row) to large-grained (~ 1μm), annealed SnS thin films at 400°C in H_2S atmosphere (bottom row).

HT treatments, however, may also cause voids and cracks in the polycrystalline SnS thin films due to locally unfavorable surface energetics and/or coefficients of thermal expansion. The SEM of the annealed SnS thin films suggest some void formation along grain boundaries. The simplified schematics on the left illustrate the effect of HT treatment on the thin film morphology. The as-deposited film at low temperature (LT, here 240°C) is densely packed, forming a continuous film. The annealed film at HT exhibits discontinuities due to the formation of holes, cracks and/or

isolated voids upon grain growth. Note that these discontinuities upon HT treatment have been observed in SnS thin films independent of the deposition technique (thermal evaporation and atomic layer deposition).[25]

When depositing the ALD *n*-type buffer material post absorber treatment, it may fill voids in the underlying HT absorber bulk, providing direct current pathways between the Mo back contact and the *n*-type buffer layer. ALD is known to provide conformal coating even in high-aspect ratio gaps and trenches.[26] In the traditional device architectures as used in reference [14], the choice of buffer layer is thus limited to semi-insulating materials. To enable the use of more conductive buffer layer materials, which may promote beneficial interface band bending in the absorber layer, we develop a simple approach to fill voids in the HT SnS bulk. We propose the deposition of a thin, continuous SnS overlayer prior to the buffer deposition. We process the second, thin SnS overlayer (75 nm) *via* ALD and at a lower temperature (120°C) to grow densely packed small SnS grains.

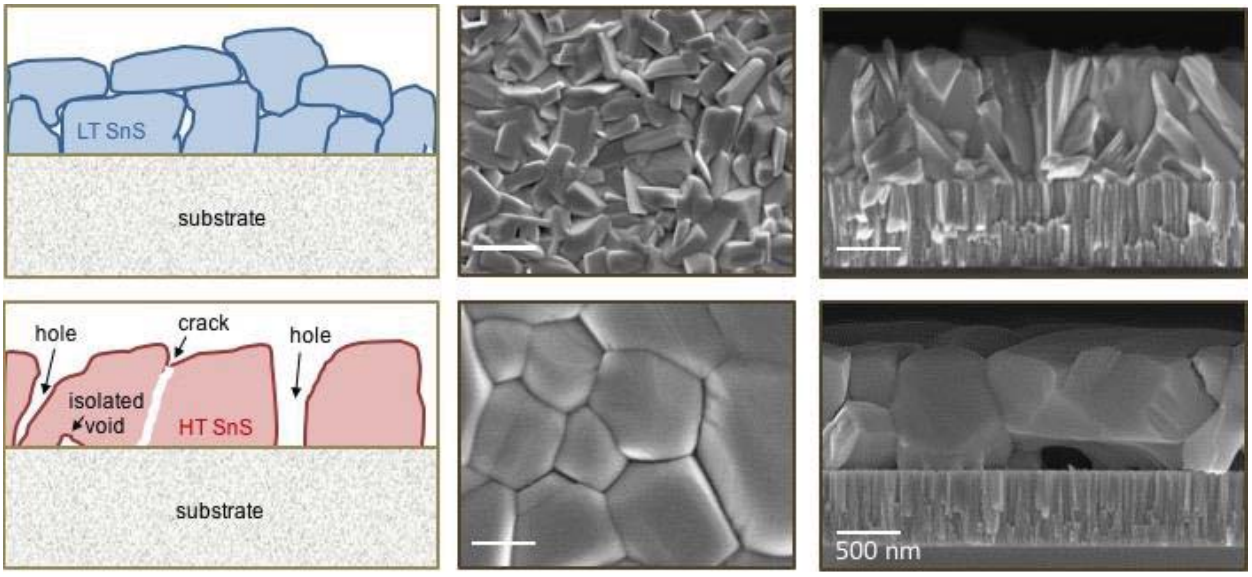

Figure 2 Morphology comparison of as-deposited SnS thin films at 240˚C (top) and sister samples annealed at 400˚C in an H_2S atmosphere. The left: simplified schematics comparing dense packing of smaller grains (< 500 nm) at low-temperature (LT) and grain growth as well as void formation at high-temperature (HT). The right: SEM in plan-view and cross-section of SnS thin film before and after H_2S annealing at 400˚C. The scale bar is 500 nm.

3.2.Two-step absorber deposition approach

We use cross-sectional SEM and EBIC to visualize the impact of the two-step deposition approach on pinhole-filling and device shunting. Results are compared to the one-step deposition baseline device. Figure 3 reveals device cross-sections of a representative one-step deposition baseline device (Figure 3a) and a representative two-step deposition device (Figure 3b). The SEMs on the left reveal cracks in the annealed SnS bulk in both devices. For the baseline device, the EBIC data shows current collection along the entire length of the crack, implying that the crack in the baseline device becomes a through-thickness current pathway, reducing the shunt resistance of the device. In the two-step deposition device, however, the LT SnS overlayer appears to successfully coat the bottom of the crack in the HT SnS bulk, preventing a detrimental through-thickness current

pathway. The EBIC data in Figure 3b suggests that the crack is only partially filled by the LT SnS. We detect no through-thickness current in EBIC at the location of the through-thickness crack in the two-step device.

Note that Figure 3 shows only a small area of each device, focusing on a representative crack between two large SnS grains. We compared the cross-section of each representative device over a lateral distance of 500 µm. In total we observe ten cracks in the SnS absorber layer in the one-step deposition baseline device and six cracks in the two-step absorber deposition device, which may contribute to the device leakage current. In the one-step deposition device, we identify five out of the ten cracks as performance limiting through-thickness current pathways. In the two-step deposition device, however, we observe only one through-thickness current pathway out of six detectable cracks. Based on the present EBIC data, the likelihood of cracks resulting in through-thickness current pathways is reduced from 50% to 16%. Table I summarizes the numbers of cracks and through-thickness current pathways for both device types.

The EBIC data indicate a lower through-thickness crack density and lower through-thickness currents in the two-step absorber deposition devices. Since EBIC is a powerful but time-intensive measurement technique, the data presented here do not provide enough statistics to quantify fully the impact of the two-step deposition approach on device shunting, but rather shows a relative comparison within the studied device areas.

Table I The numbers of cracks and through-thickness current pathways in the SnS absorber bulk that are observed in a representative one-step deposition device and two-step deposition device across a total lateral distance of 500 µm.

Device architecture	# of detectable cracks (SEM)	# of through-thickness current pathways (EBIC)
One-step deposition	10	5
Two-step deposition	6	1

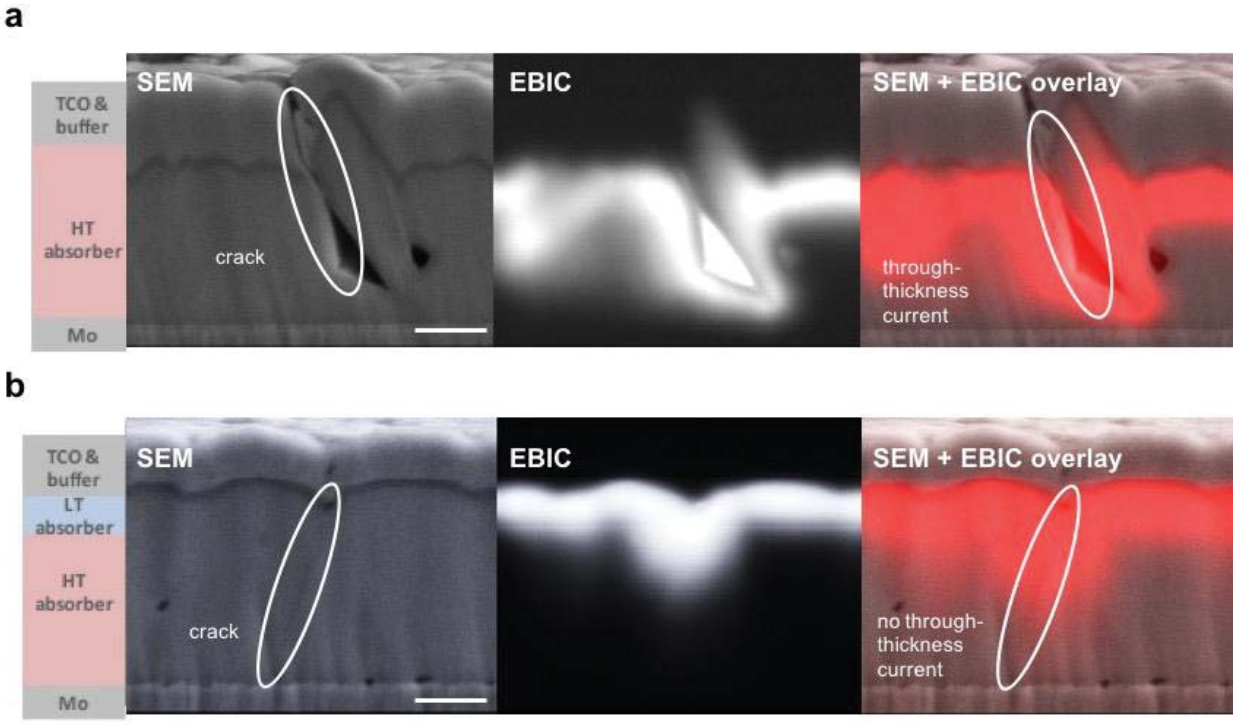

Figure 3 Cross-sectional SEM and EBIC measurements of SnS substrate-style devices. **a** one-step absorber deposition with high-temperature (HT) treatment as applied in the baseline SnS substrate-style device architecture. Cracks in the annealed SnS bulk become preferred through-thickness current pathways, creating pathways of lower resistance between the Mo back contact and the buffer layer and transparent conductive oxide (TCO) on top, as demonstrated in the EBIC image. **b** two-step absorber deposition approach employing a second, thin SnS overlayer deposited *via* ALD at low-temperature (LT) to fill voids in the HT SnS bulk and to prevent detrimental through-thickness current pathways. Despite the appearance of a crack in the absorber layer, there is no through-thickness EBIC signal that would indicate a shunt pathway. The scale bar is 400 nm.

3.3.Tin sulfide solar cells

Next, we performed current density–voltage (*J-V*) measurements on eleven identically processed SnS one-step deposition baseline devices and two-step deposition devices. The distribution of *J-V* curves measured in the dark and under 1 Sun illumination is shown in Figure 4a and 4b. While both sample sets—baseline (red lines) and two-step deposition (blue lines)—contain one heavily shunted cell each, we observe a broader performance spread across the baseline cells. In Figure 4c, we compare the *J-V* curves of one representative one-step deposition baseline device (red lines) and one two-step deposition device (blue lines), indicating a high V_{OC} of 370 mV and a low leakage current density of 18 nA/cm^2 in short-circuit condition for the two-step deposition device. The solar cell characteristics of the two representative devices from Figure 4c are listed in Table II. Both devices were measured under similar conditions without a light mask at MIT. We observe a 5.6% relative improvement in the V_{OC} and 5.1% relative improvement in the FF for the two-step deposition device compared to the one-step deposition baseline device due to improvements in the shunt resistance R_{sh} by more than a factor of 3.5 under illumination and a factor of 30 in the dark. The J_{SC} of the two-step deposition device, however, is 3.7% lower relative to the one-step

deposition device. The overall device efficiency reveals a slight improvement by 7% relative from 3.80% to 4.08% experimentally (see Table II).

An independent *J-V* measurement on the representative baseline device was performed at NREL with and without light mask, indicating a 2 – 3% relative decrease in V_{OC} and J_{SC} and a 2 – 3% increase in the FF, when applying the light mask. Comparing the measurements at MIT and at NREL suggests that the J_{SC} measurements at MIT yield an 8.5% overestimate. The V_{OC} and FF measurements at MIT and NREL without light mask are within the statistical error.

The shunt resistance R_{sh} was computed from the dark and illuminated *J-V* data in reverse bias for nine identically processed baseline and two-step deposition devices. We compare the light R_{sh} for the HT baseline and the HT+LT two-step deposition device in Figure 4d. We exclude two baseline and two-step deposition devices due to heavy shunting because we attribute the shunting in these cases to macroscopic shunts formed during sample handling. The median light R_{sh} improved from 129 Ω cm^2 for the one-step baseline devices to 469 Ω cm^2 for the HT+LT two-step deposition devices (> factor of 3.5). The median dark R_{sh} improved from 134 Ω cm^2 to 3997 Ω cm^2 (factor of 30).

For the HT+LT device, we observe a R_{sh} reduction (factor of 8.5) upon illumination, which hints at some voltage-dependent collection efficiency. Note that the HT SnS bulk and the LT SnS overlayer are processed *via* different deposition techniques (thermal evaporation and atomic layer deposition) as well as at different temperatures. This may affect charge collection at the SnS absorber/buffer interface. Overall, the narrower distribution of the light R_{sh} indicates an improved performance reproducibility for the HT+LT devices with standard errors σ_{Rsh} of 21 Ω cm^2 compared to 34 Ω cm^2 for the baseline devices.

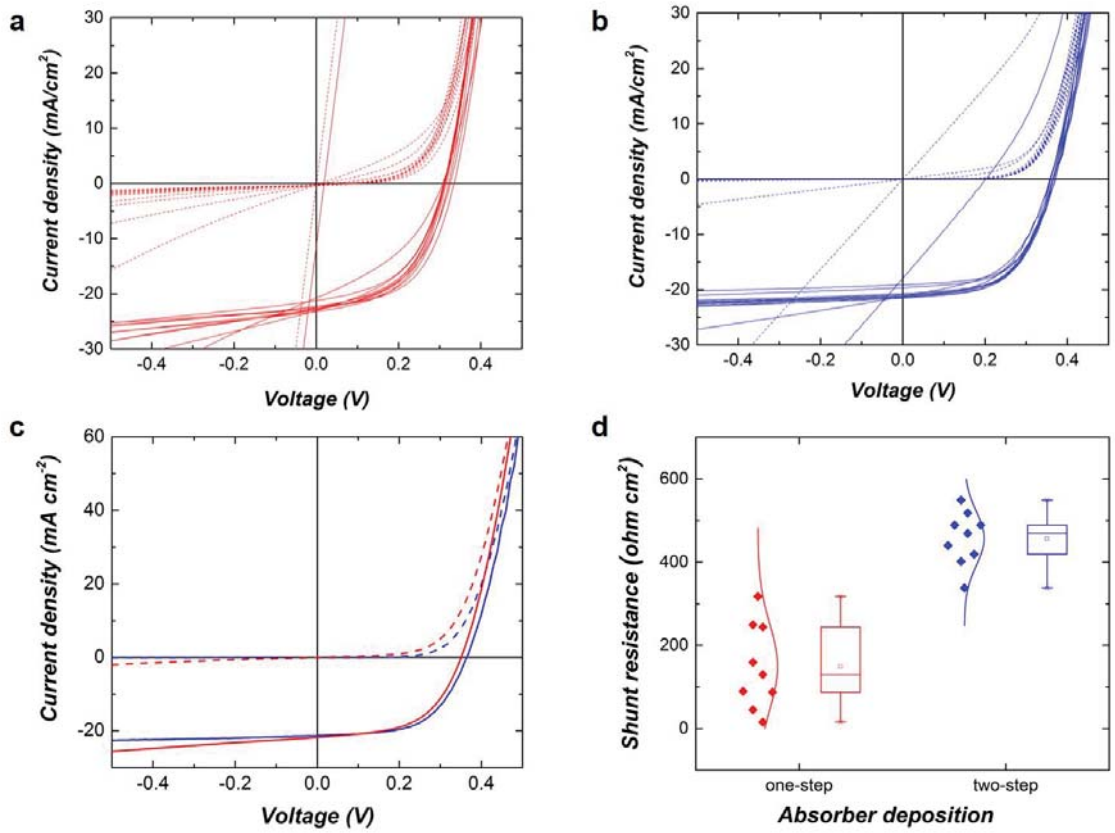

Figure 4 Comparison of SnS solar cell data of the baseline device which includes a high-temperature (HT) absorber treatment and the two-step absorber deposition device which uses a low-temperature (LT) absorber overlayer on top of the HT treated absorber bulk. **a** and **b** show the distribution of *J-V* characteristics in the dark (dashed lines) and under 1 Sun illumination (solid lines) for eleven identically processed devices following the baseline processing protocol (plot **a**, red lines) and the two-step absorber deposition (plot **b**, blue lines), respectively. **c** directly compares the *J-V* data of two representative devices (baseline HT and two-step deposition HT+LT). **d** compares the illuminated shunt resistance R_{sh} of the baseline HT and two-step deposition HT+LT SnS devices, excluding heavily shunted devices.

Table II Solar cell device data for the representative one-step deposition baseline and two-step deposition device characterized at MIT and at NREL, with and without light mask.

Device	Facility	Light mask	V_{OC} [mV]	J_{SC} [mA/cm^2]	% FF	% PCE
One-step dep.	MIT	No	350.8	19.9	54.3	3.80
Two-step dep.	MIT	No	370.6	19.2	57.1	4.08
One-step dep.	NREL	No	351.9	20.0	53.5	3.78
One-step dep.	NREL	Yes	342.5	19.5	55.0	3.69

4. Summary and Conclusions

In this work, we have developed a simple approach to mitigate shunt losses in thin film solar cells that may result from pinhole formation in polycrystalline materials. By engineering a two-step absorber deposition method, we demonstrate a robust substrate-style device architecture, which

appears to successfully eliminate through-thickness current pathways in the polycrystalline absorber bulk.

We test this approach on tin sulfide (SnS) thin film solar cells as a proof-of-concept. The two-step deposition yields a more than 3.5x superior device shunt resistance under illumination compared to the more standard approach of using a semi-insulating buffer layer directly on top of the annealed absorber bulk. Improvements in the shunt resistance are correlated to gains in the open-circuit voltage and fill factor, resulting in an overall device performance improvement from 4.15% to 4.44% (both devices measured at MIT). Even more importantly, the newly engineered devices, incorporating the two-step absorber deposition, reveal higher performance reproducibility.

It is worth noting that the baseline devices used in this study were initially fabricated and characterized at MIT in February 2014. The here presented data in Figure 4c and Table II, however, were taken in March 2016 at MIT and NREL. Comparing the data sets from 2014 (see reference [14]) and 2016, we do not observe any evidence of materials degradation despite ambient air exposure for 24 months.

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